

IN THE UNITED STATES  
PATENT AND TRADEMARK OFFICE

Patent Application

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Case: 3-6-16

Serial No.: 09/653,295

Filing Date: August 31, 2000

Examiner: Nguyen

Group Art Unit: 2811

Title: Stacked Structure For Parallel Capacitors And Method Of  
Fabrication

ASSISTANT COMMISSIONER FOR PATENTS  
WASHINGTON, D. C. 20231-

SIR:

Request For Reconsideration After Final Rejection  
Request for Removal of Final Rejection Under 37 C.F.R. §1.113

This paper is in response to the final office action mailed August 26, 2002.  
For reasons provided herein it is respectfully requested that the examiner  
withdraw the finality of the office action and pass the application to issuance.

Claims 1-10 are pending in the application. Claims 7-10 are withdrawn as  
subject to a restriction requirement which has been twice traversed. A second  
request for withdrawal of the restriction requirement is included with this  
response.

Claims 1-6 have been rejected under section 103 over Saia in  
combination with Watanabe and Roy. At the outset, it is noted that the examiner  
previously rejected applicants' claims under section 103 based on Arai in

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combination with Watanabe and Sala. In response, the claims were amended to more clearly direct the inventive subject matter to a monolithic integrated circuit. Apparently, the examiner agrees that Arai does not, alone or in combination with other art of record, provide necessary disclosure to meet the terms of applicants' claims. The Arai reference was directed to a hybrid or composite. In contrast, the claimed invention is directed to a monolithic integrated circuit device. It has been noted for the examiner's benefit that the "first and second levels of interconnect conductor" of claim 1 are a portion of the claimed monolithic integrated circuit device. In response, the examiner withdrew the rejection based on the Arai reference.

Now, however, the examiner substitutes the Saia reference for the Arai reference in order to finally reject applicants' claims. Unfortunately, the Saia reference has deficiencies similar to those of the Arai reference. Specifically, the examiner mistakenly urges that Saia discloses a monolithic integrated circuit at column 2 lines 24-27. This is not at all the case. The referenced passage only describes fabricating "an integral multi-layer thin film capacitor on a polymer layer using staggered via landing pads."

If the examiner reviews other portions of the reference the deficiencies under section 103 will be readily apparent. Specifically, it is made clear throughout column 1 that Saia deals with high density integrated circuit modules (see lines 1-2) and formation of capacitors on polymer layers (see line 66). There is simply no teaching in this reference for the formation of capacitor structures in a monolithic integrated circuit. Accordingly, because the

combination fails to meet the requirements of the claims, the claims are allowable over the art of record and allowance is therefore requested. If the examiner disagrees or would like to discuss technical details of the references or the invention, the examiner is invited to telephone the undersigned.

With regard to the erroneous restriction requirement, the examiner has urged that in the prior office action it was "clearly" pointed out "that there is a method other than the method in the present invention to produce the claimed structure." If the examiner had ever clearly pointed out a correct basis for the restriction requirement, the undersigned would not continue to disagree. It has already been suggested that if the examiner still disagrees with the undersigned's position that the examiner should confer with his supervisor, Mr. Tom Thomas, to discuss the merits of the restriction requirement. Again, it should be noted that the broadening of a claim by removal of a step does not result in creation of a different species of that claim.

Accordingly, it is requested that the examiner immediately review the withdrawn claims, and, if appropriate, further search the subject matter of claims 1-10 since none of the art of record is sufficient for rejecting any of applicants' claims. Applicants request that the examiner endeavor to do so in order to ensure a more thorough investigation of the invention.

For all of the above reasons it is requested that finality of the office action be withdrawn, all of the claims be examined and that the examiner respond to the undersigned within two weeks of receiving this response.

Respectfully submitted,

By Ferdinand M. Romano  
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Date: 28 October, 2002

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